RGB LED Cluster Driver Data sheet NU801

3 channel 16 bit PWM Constant Current Driver

Features

- 3 adjustable constant current sink channel
- 16 bit high resolution PWM output
- Built-in 60MHz PWM oscillator
- Non-scrambled 910Hz PWM refresh rate
- 3mA ~ 200mA channel driving capability
- 0.8V (200mA/channel) low output voltage dropout
- Picture motion blur elimination talent
- 2 or 3 wire data transmission technology
- Maximum 8MHz serial in clock frequency
- 3V ~ 24V wide range power supply voltage
- 0V ~ 26V output channel sustain voltage
- Automatic power down function
- Built-in 20mA/5V voltage output
- 160℃ junction temperature thermal shutdown
- Less than 0.5%/10℃ thermal regulation
- Less than 5% chip current skew
- Less than 3% channel to channel current skew
- Less than 1%/V line regulation
- Less than 1%/V load regulation
- Green package

Applications

- Outdoor/Indoor LED mesh display
- General LED Lighting
- Decoration lighting for architecture
- Landscape lighting
- Ground / Wall indicator
- Ambient Lighting
- High speed PWM generator

Package Type & Part No.

Part No.	Package type
NU801SS	SSOP 150 mil 16 pin

Protection

- 8KV ESD protection circuit

Product Description

NU801 is a high performance PWM-embedded 3 channel constant current LED driver with high speed, high grey level resolution, high current linearity, high driving capability and wide supply voltage range. It incorporates shift registers and data latches for control data transmission in cascade pixel or light source system. All these special characteristics make NU801 very suitable for wide area LED display and various lighting applications.

For the display application, the current of LED can be driven precisely by embedded 16 bit PWM controller. That can keep picture clear when the brightness is quite low. In contrast to scrambled PWM output, the 910 Hz non-scrambled PWM output of NU801 not only keeps the high refresh rate but also minimizes the EMI generation and current distortion while output is switching. Furthermore, NU801 supports easy 2-wire data transmission interface that can reduce the firmware complexity, lower the BOM cost and enhance system reliability.

A special picture motion blur eliminating function (patent granted) is provided by NU801. Whenever the content of display updated, the data latch action will temporary disable all output channel. The special innovative design will naturally eliminate the visual staying phenomenon for fast moving object on screen.

For the lighting application, each output channel can drive current up to 200mA. Therefore, in a 24V power system, maximum about 13 watt LEDs can be driven by a single NU801. To keep NU801 output constant, at least 0.8V operation voltage drop in current path is required. NU801 adopts in path resistor structure to control the output current. The portion of voltage drop on NU801 is 0.5V and the other 0.3V drop is on external in path current setting resistor. The in path resistor structure will lower the heat generation from NU801 and let the lighting system more reliable.

In order to cooperate with other wise controller such as MCU or some peripheral devices, NU801 can provide a 5V voltage source. For some special stand alone systems, this feature can simplify the power regulation circuit, reduce the size of system and greatly expand the flexibility of system integration.

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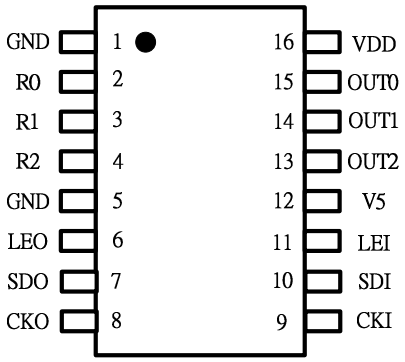
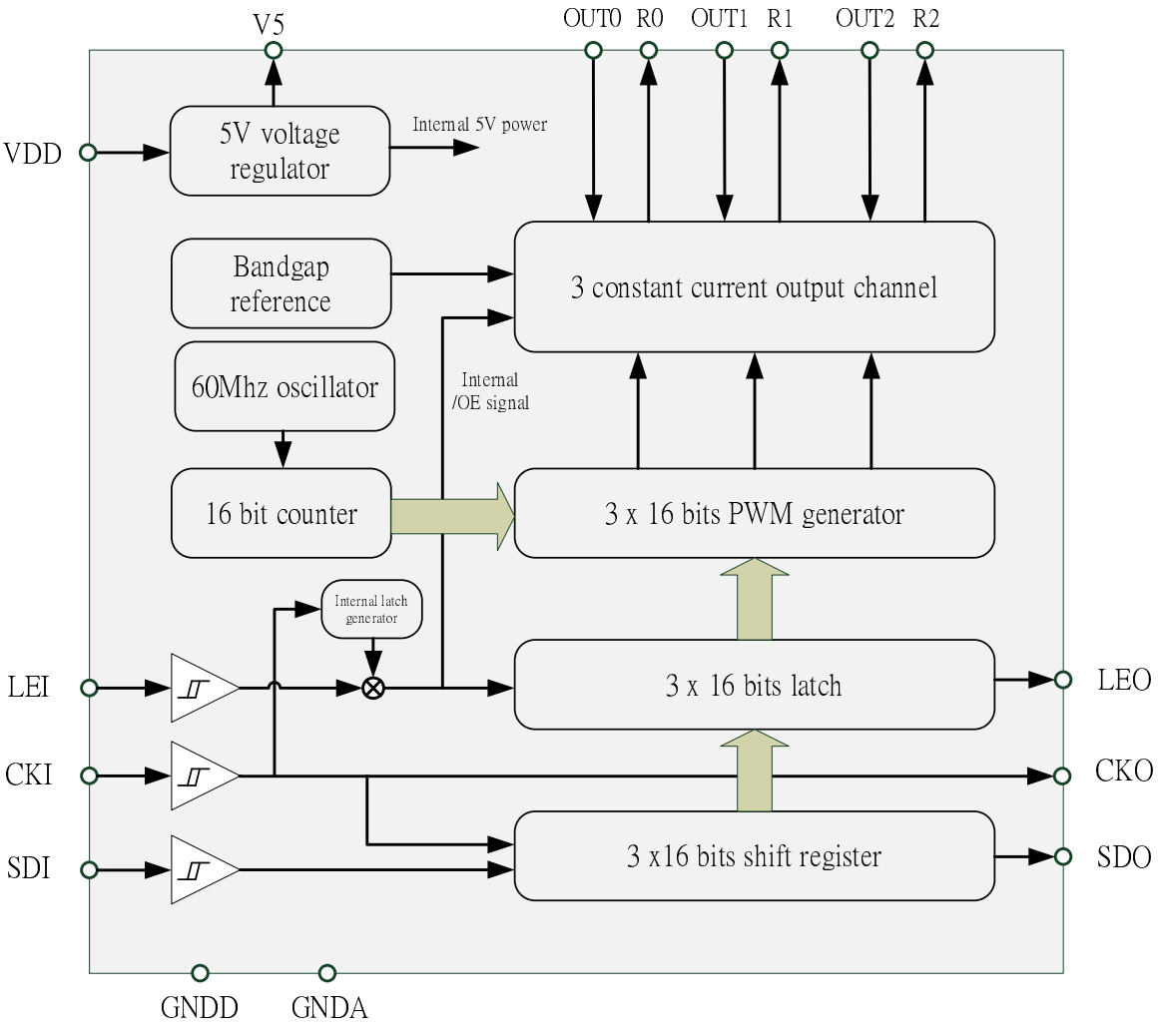
Pin Configuration & Terminal Description



Pin #	Pin name	Function
1	GND	Ground
2	R0	Channel 0 current set resistor
3	R1	Channel 1 current set resistor
4	R2	Channel 2 current set resistor
5	GND	Ground
6	LEO	Latch enable output
7	SDO	Serial data output
8	CKO	Clock output
9	CKI	Clock input
10	SDI	Serial data input
11	LEI	Latch enable input
12	V5	5V power supply output
13	OUT2	Output channel 2
14	OUT1	Output channel 1
15	OUT0	Output channel 0
16	VDD	Power supply

Block Diagram



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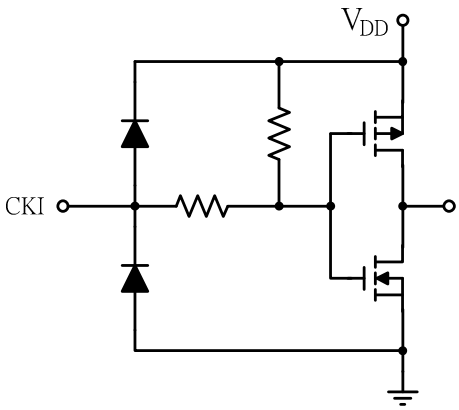
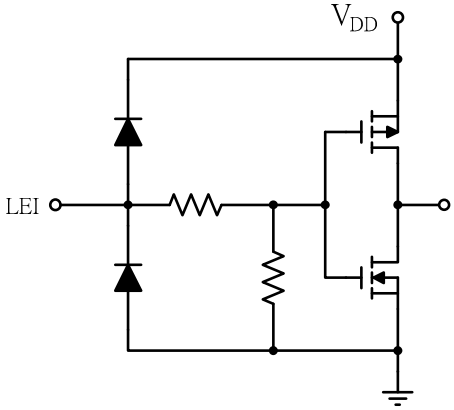
Equivalent Circuits for Inputs and Output

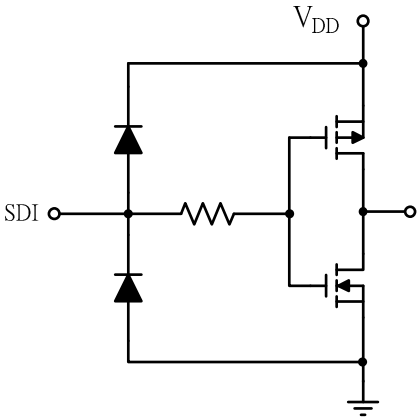
- **Clock terminal**



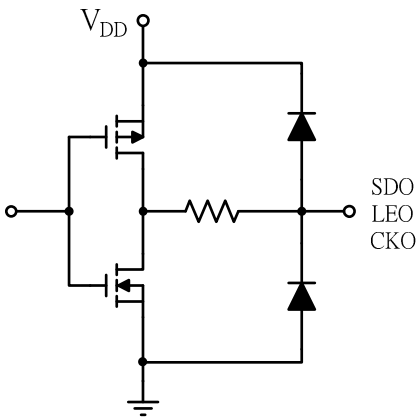
- **Latch Enable terminal**



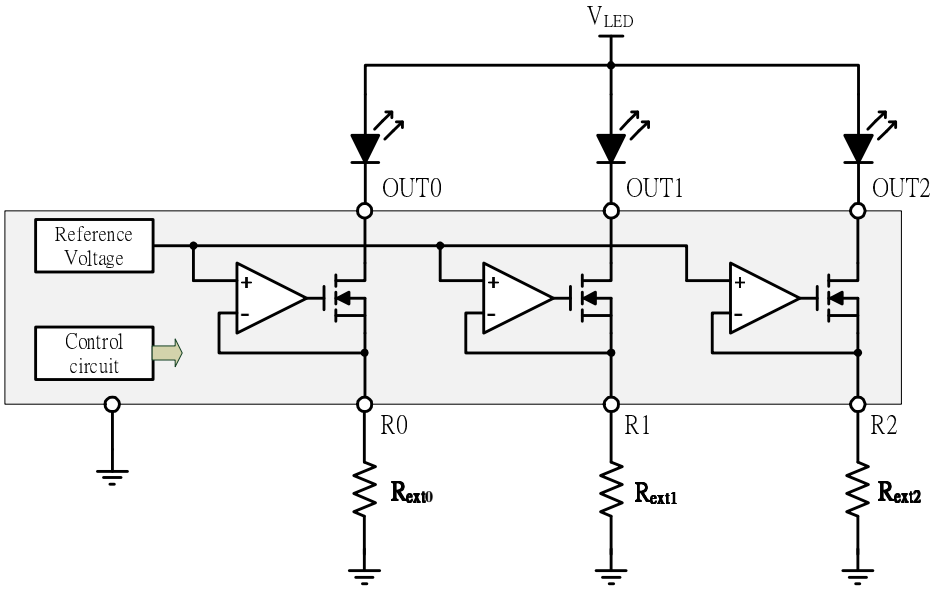
- **Serial Data Input terminal**



- **Serial Data / Latch Enable / Clock Output terminal**



- **Output / R_{EXT} terminal**



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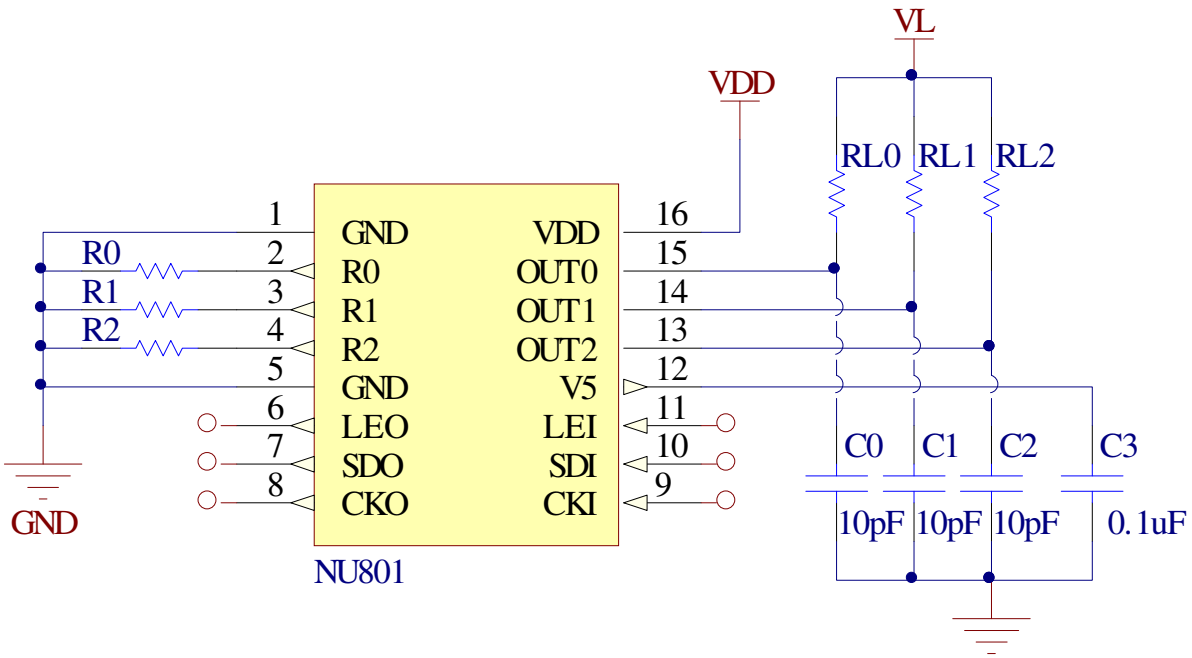
Maximum Ratings (T = 25°C)

Characteristic	Symbol		Rating	Unit
Supply voltage	V_{DD}		0 ~ 24	V
Output channel voltage	V_{OUT}		-0.2 ~ 28	V
Output current per channel	I_{OUT}		3 ~ 250	mA
Input voltage (Digital I/O)	V_{OE}		-0.2 ~ V_{DD}	V
Output voltage (Digital I/O)	V_{DIO}		0V / 5V	V
Power Dissipation (On PCB)	P_D	SOP	0.86	W
		SSOP	0.82	
		QFN	2.0	
Thermal Resistance	$R_{TH(j-a)}$	SOP	110.9	°C /W
		SSOP	115.9	
		QFN	37.14	
Operating temperature	T_{OPR}		-40 ~ +85	°C
Storage temperature	T_{STG}		-55 ~ +150	°C

Test Circuit



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Electrical Characteristics and Recommended Operating Conditions

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	Room Temp.	3	5	24	V
Supply current	I_{DD}	V_{DD} = 5V	1.6	2.7	3.5	mA
	I_{DD}	All PWM output off (Power down mode)	35	-	150	uA
Output drop out voltage	V_{OUT}	V_{DD} = 5V, I_{OUT} = 20mA	0.5	-	24	V
		V_{DD} = 5V, I_{OUT} = 80mA	0.6	-	24	V
		V_{DD} = 5V, I_{OUT} = 200mA	0.8	-	24	V
Output current	I_{OUT}	-	3	-	200	mA
Output breakdown voltage	V_{OUT}	-	24	-	30	V
R_{EXT} Output voltage	V_{Rext}	V_{DD} > 3V	-	0.38	-	V
Bit current skew	dI_{OUT1}	I_{OUT} = 150mA, V_{OUT} = 1 V	-	±1	±3	%
Chip current skew	dI_{OUT2}	I_{OUT} = 150mA, V_{OUT} = 1 V	-	-	±5	%
Leakage	$I_{Leakage}$	V_{OUT} = 24V	-	-	0.5	uA
Clock Frequency	F_{CLK}	V_{DD} >= 5V, 40% < Duty < 60%	-	-	8	MHz
5V voltage regulator	V5	V_{DD} >= 5.2V, I_{v5} = 0mA	4.2	5	5.2	V
		3V < V_{DD} < 5.2V, I_{v5} = 0mA	V_{DD} - 0.2	-	V_{DD}-0.05	
	I_{v5out}	V_{DD} > 5V, V5 > 4V	20	-	-	mA
I/O Input voltage	V_{IH}	V_{DD} >= 5V	2.4	-	-	V
	V_{IL}	V_{DD} >= 5V	-	-	1.5	
I/O output voltage	V_{OH}	I/O current = -5mA	4.5	-	5	V
	V_{OL}	I/O current = 5mA	0	-	0.5	
Pull up resistor (Clock)	R_{PU}	-	900	1100	1400	KΩ
Pull down resistor (OE)	R_{PD}	-	500	750	1000	
Output Line regulation	$\%/V_{DD}$	3V < V_{DD} < 24V	-	-	1	△I%/V
Output Load regulation	$\%/V_{OUT}$	0.6V < V_{OUT} < 8V	-	-	1	△I%/V
Output Thermal regulation	%/10˚C	3V < V_{DD} < 24V	-	-	0.3	△I%/10˚C
Operating Temperature	T_{OPR}	Ambient temperature	-40	-	85	˚C
Junction Temperature Thermal Shutdown	T_{Shut}	All output off	-	160	-	˚C

Switching Characteristics (T = 25˚C)

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay ('L' to 'H')	LE - OUTn	t_{pLH1}		50	80	120	nS
	CKO - SDO	t_{pLH2}		-	15	-	
	LEI – LEO	t_{pLH3}		-	25	35	
	CKI - CKO	t_{pLH4}		-	34	50	
Propagation Delay ('H' to 'L')	LE - OUTn	t_{pHL1}		250	300	350	
	CKO - SDO	t_{pHL2}		-	15	-	

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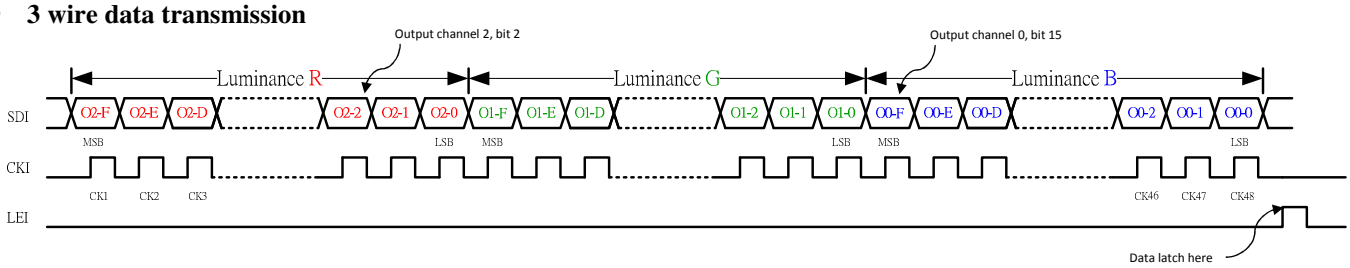
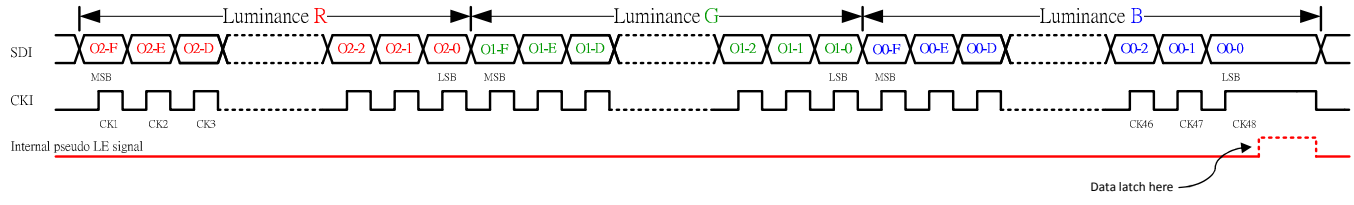
	LEI – LEO	t_{pHL3}	V_{DD} >= 5V V_L = 5V V_{IH} = V_{DD} V_{IL} = GND R_{EXT} = 2.5Ω R_L = 30Ω C_0 = C_1 = C_2 = 10 pF C = 0.1uF Temp. = 25°C	-	30	40	
	CKI - CKO	t_{pHL4}		-	25	50	
Pulse Width	$CLK_{(Clock High)}$	$t_{w(CLK)}$		0.03	-	500	uS
	$CLK_{(Clock Low)}$			60	-	-	nS
	$CLK_{(LATCH)}$			600	-	-	uS
	LE	$t_{w(LE)}$		30	-	-	nS
	CKO	$T_{CKO(Min)}$		32	-	-	nS
Maximum Clock Frequency		F_{CLKMAX}		-	-	8	MHz
Clock Latch Hold time		$t_{h(CLK)}$		500	550	600	uS
Setup time for LE		$t_{s(LE)}$		20	-	-	nS
Hold time for LE		$t_{h(LE)}$		5	-	-	
Setup time for SDI		$t_{s(SDI)}$		5	-	-	
Hold time for SDI		$t_{h(SDI)}$		5	-	-	
V_{OUT} Rising Time (driver off)		t_{or}		-	120	200	
V_{OUT} Falling Time (driver on)		t_{of}		-	120	200	
Internal OSC frequency		F_{OSC}		55	60	65	MHz
PWM frequency		F_{PWM}		840	910	990	Hz
Power Down Recovery Time		T_{Wake}	From CLK rising edge	-	-	5	nS

Luminance Data Transmission

- **3 wire data transmission**



- **2 wire data transmission**



When clock signal keep high for more than 600us, NU801 will generate an internal pseudo LE signal. That will trigger the data latch circuit to hold the luminance data.

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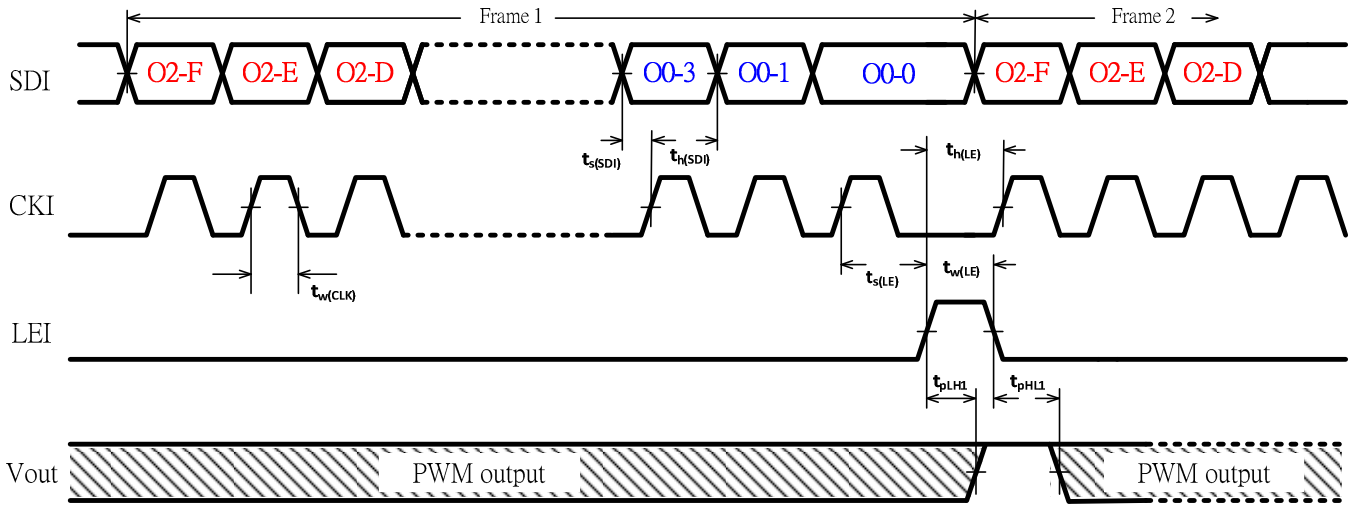
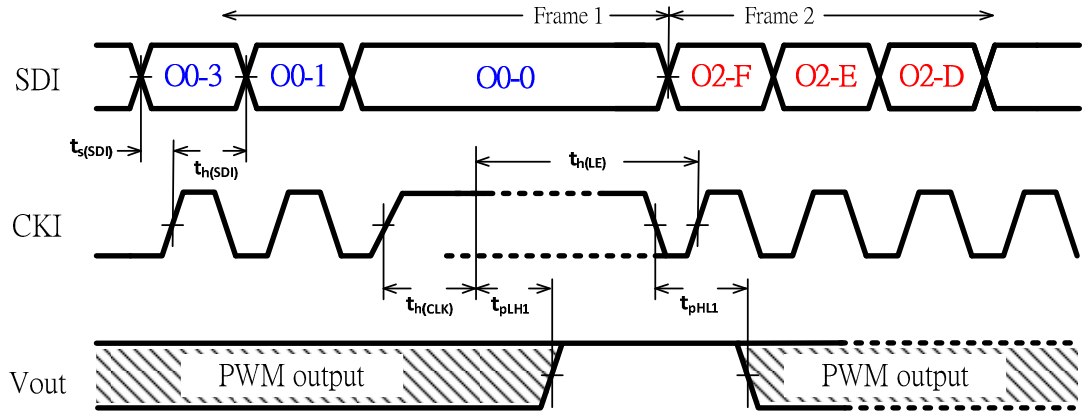
Timing Waveform

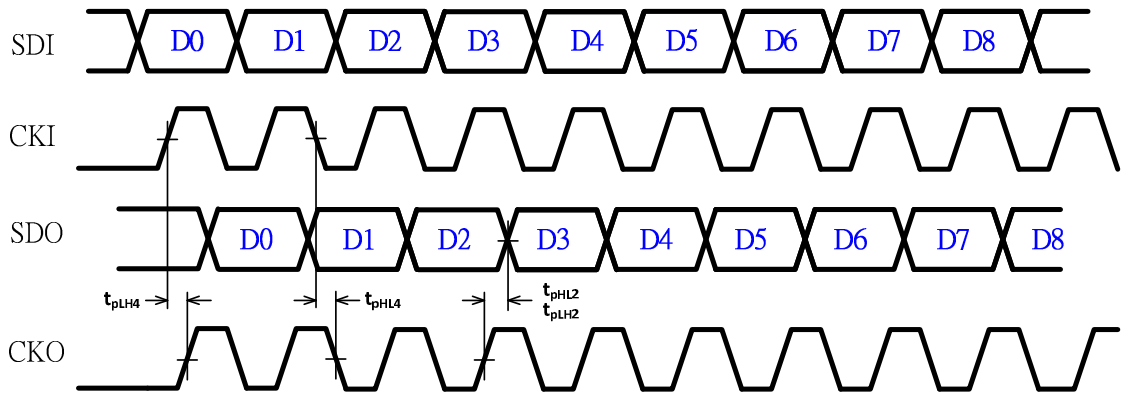
- **LE trigger data latch**



- **Clock trigger data latch**



- **Clock in - Clock out and Serial in - Serial out Propagation delay**



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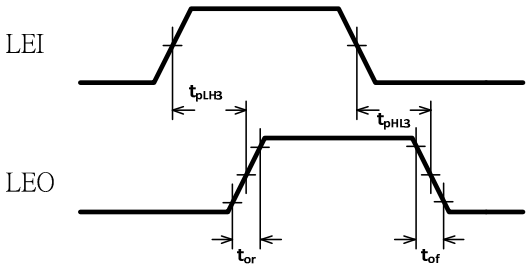
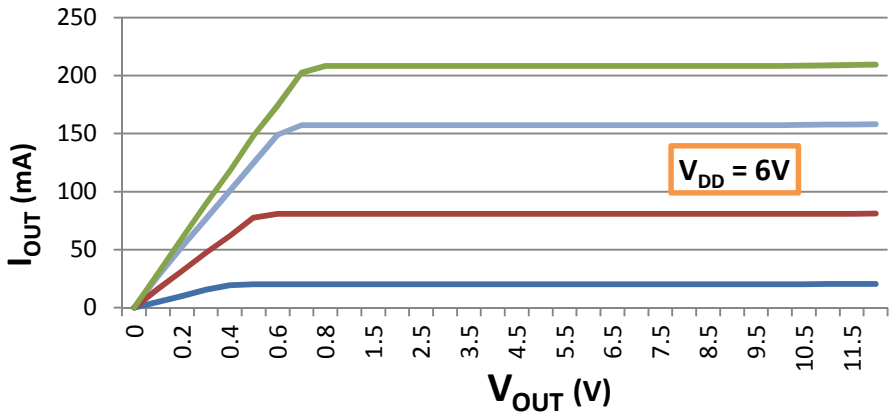
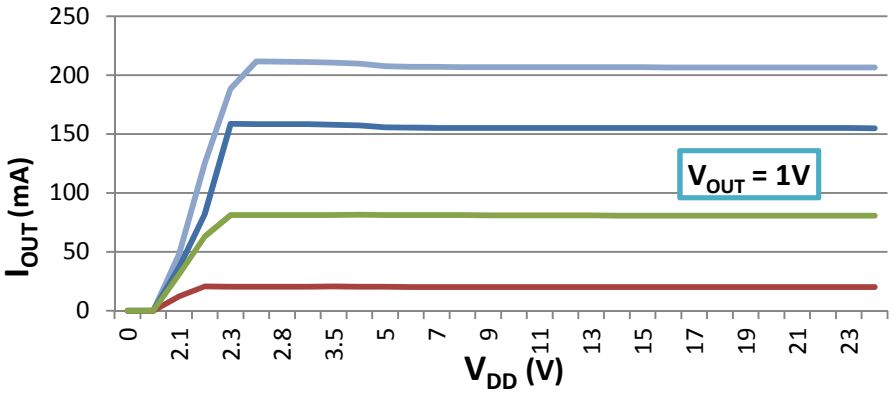
- **Latch in – Latch out Propagation delay**



Output I/V curve



Line regulation



Automatic Power Down and Recovery

The power down mode in NU801 is almost a silent function. That is, system doesn't need to do anything for this function at most time. If the system controller always updates all luminance data of whole system each time the screen updated, there is nothing should be care about. But if controller updates partial luminance data of whole system each time, a 5uS or longer leading clock pulse for first data bit should be implemented. This longer clock will compensate the wakeup time of those NU801 which is in power down mode.

The NU801 will get into power down mode automatically when all-zero luminance data (Luminance data of three output channels are all zero) is set and leave this mode by triggering from next clock rising edge. Although the first clock rising will resume the internal shift register immediately, but there are about 4us wakeup time for CKO regeneration control circuit.

Once the power mode activated, the I_{DD} current will lower down at about 80uA for energy saving. This unique power down function can save the system power dynamically even when system is in working state.

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Picture motion-blur elimination

To eliminate the motion blur of moving picture on screen, the content on screen must be temporary shut off for a while when the content on screen is changed. In NU801, the *LE* signal is equal to $\overline{OE}$ signal. When the new luminance data is latched by *LE* signal, this logic high *LE* ($\overline{OE}$) signal will shut off all output channel. The system controller can control the duration of *LE* ($\overline{OE}$) signal to obtain the desire time interval for the motion blur elimination. After the *LE* ($\overline{OE}$) signal is back to logic low, the new luminance data is updated and all outputs are back to work. The *LE* ($\overline{OE}$) signal is not only coming from the LE pin but also come from clock. When clock keeps logic high for more 600us, an internal *LE* signal will be generated. This internal *LE* signal has same effect like *LE* signal from external LE pin.

Output Current Setting

The output current of NU801 is set by an external resistor (R_{EXT}). The current of each output channel can be calculated by the equation following.

$$I_{OUTn} \cong \frac{0.38}{R_{EXT_n} + 0.2\Omega}$$

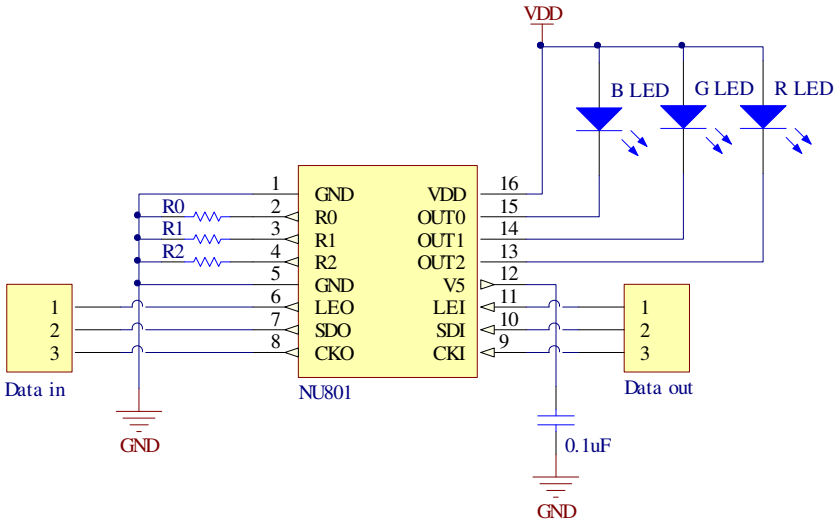
Typical application circuit

$$I_{OUTn} = \frac{0.38}{R_{EXTn} + 0.2\Omega}$$

V_{DD} = 3 ~ 24V

$V_{OUTn} = V_{DD} - V_{LEDn}$

$$P_D \fallingdotseq I_{out0}*(V_{out0} - 0.38) + I_{out1}*(V_{out1} - 0.38) + I_{out2}*(V_{out2} - 0.38)$$



Application Note

- In order to keep each output current uniform, the routing path of $Rext_n$ on PCB should be taken care. Because the parasitic resistance on these routing paths will influence the channel output current. The path from R_n terminal to $Rext_n$ of three channels should be kept the distance and width as same as possible. That will let the parasitic resistance of three channels are same. On the other side of three $Rext_n$ are connected together and link to the ground pins of NU801. This ground net should be shorter and wider for higher current passing through and keep the voltage drop minimized that will greatly improve the current skew between NU801s.
- There are two GROND pin within NU801. Both pin should be connected together on PCB to keep NU801 function normal.
- For the sake of noise immunity on V_{DD} pin, it is suggest that a 0.1uF capacitor is connected between V5 and GND pin.
- When using 2 wire transmission method, LE pin should be connected to GND pin or leave it floating.
- In order to minimize the heat generation from NU801, the proper V_{DD} voltage should be chosen carefully to keep V_{OUTn} as low as possible when that output channel is turned on.

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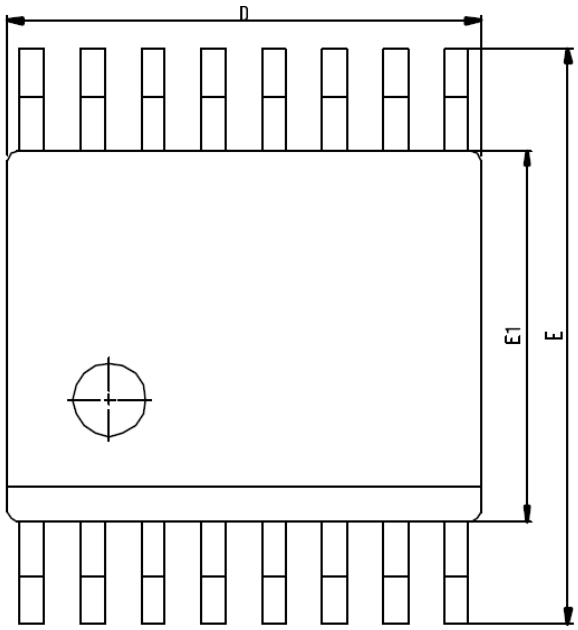
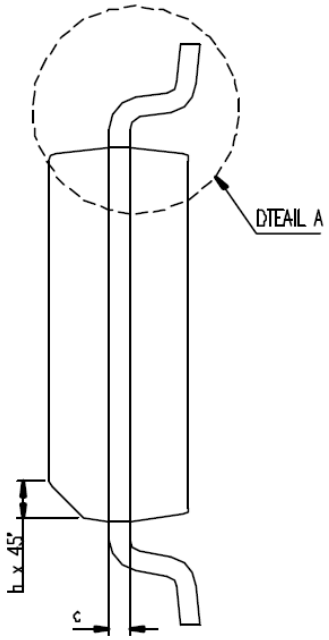
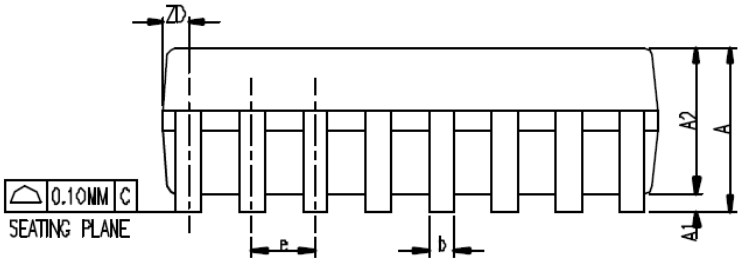
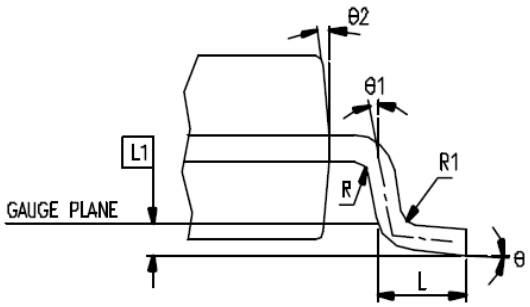
Package Dimensions

- **SSOP16L 150 mil**









SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			1.50			0.059
b	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e	0.635 BASIC			0.025 BASIC		
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
h	0.25		0.50	0.010		0.020
L1	0.254 BASIC			0.010 BASIC		
ZD	0.229 REF			0.009 REF		
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
θ	0°		8°	0°		8°
θ1	0°			0°		
θ2	5°	10°	15°	5°	10°	15°
JEDEC	MO-137 (AB)					

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